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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/183,694 10/30/98 ELLIS

J 98-179

EXAMINER

TM02/0516

LSI LOGIC CORPORATION  
1551 McCarthy Blvd., MS: D-106  
Patent Law Department  
Milpitas CA 95035

PARK, I

ART UNIT

PAPER NUMBER

2182

DATE MAILED:

05/16/01

13

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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# Office Action Summary

Application No.

09/183,694

Applicant(s)

ELLIS ET AL.

Examiner

Ilwoo Park

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

## Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some \* c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☐ received.
2. ☐ received in Application No. (Series Code / Serial Number) \_\_\_\_\_.
3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 12.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_.

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### DETAILED ACTION

1. Applicant's amendment filed on 3/5/2001 in response to Examiner's Office Action has been reviewed. Claims 1, 2, 4, 9, and 11-15 are amended. The following rejections now apply.
2. Claims 1-20 are presented for examination.
3. Garrett et al., Born et al., Krakirian, and Bass et al. were cited as prior art in the last office action.
4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
5. Claims 1 and 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garrett et al., US patent No. 6,049,842 and Bean et al., US patent No. 4,543,626.

As to claim 1, Garrett et al teach a data controller (efficient data transfer mechanism) comprising:

a transfer extend generator that generates (col. 3, lines 14-15) transfer extend entries for a data transfer; and

at least one retrieval channel coupled to receive (col. 3, lines 42-43) the transfer extend entries for programming (col. 4, lines 4-6) the data transfer.

However, Garrett et al do not teach the data controller located within a peripheral device having a storage medium for data transfer between the storage medium and a host.

Bean et al teach a data controller of a peripheral device (fig. 1) having a storage medium for data transfer between the storage medium and a host. Specifically, Bean et al teach a data

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transfer using transfer extend entries generated by the data controller located within the peripheral device from a host commands received.

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Garrett et al and Bean et al because they both teach a data transfer using transfer extend entries and the Bean et al's teaching of the data controller located within a peripheral device would increase flexibility in adapting host without the specific driver.

As to claims 5-8, the reasons set forth in the last office action are incorporated herein by reference.

As to claim 9, Garrett et al teach the status retrieval channel monitors (col. 4, lines 32-35) a data transfer between a buffer memory (FIFO 25) and a storage medium (memory 12). And Bean et al teach a data transfer between a buffer memory (data memory 26) in the peripheral device and the storage medium (disk/tape 30, 32).

As to claim 10, Bean et al teach the data controller is coupled to a first storage device that stores the transfer extend entries (col. 4, lines 8-14).

As to claim 11, Bean et al teach the retrieval channel provides used read pointers to the first storage device for reuse (implicit: col. 7, lines 29-57).

6. Claims 2, 3, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellis et al., US patent No. 6,029,226.

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As to claim 2, Ellis et al teach a data controller (col. 4, lines 38-58) of a peripheral device having a storage medium and a processor, wherein the data controller minimizes (col. 7, lines 1-3) interrupts to the processor by processing a plurality of sequential commands (col. 6, lines 17-33; col. 6, lines 63-66) received from a host computer.

As to claim 3, Ellis et al teach a data controller (col. 4, lines 38-58), that is couplable to a host and coupled to a storage medium, microprocessor, local storage and a buffer memory, comprising a command queuing engine that creates and executes threads of sequential commands (col. 6, lines 17-33; col. 6, lines 63-66) while minimizing (col. 7, lines 1-3) interrupts associated to the commands.

As to claim 12, Ellis et al teach a command queuing engine configured to arrange the plurality of sequential commands into at least one thread (col. 6, lines 17-33).

7. Claims 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis et al., US patent No. 6,029,226 as applied to claims 12 and 3 above, and further in view of Bean et al., US patent No. 4,543,626.

As to claims 13, 16, and 18, Bean et al teach a command queuing engine comprises:  
a transfer extend generator configured to generate (col. 4, lines 38-42) transfer extend entries for a data transfer between the storage medium and a host computer; and  
a data retrieval channel (col. 6, lines 64-68) coupled to receive the transfer extend entries for programming the data transfer.

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As to claims 14 and 19, Bean et al teach the command queuing engine further comprising a status retrieval channel (col. 4, lines 18-21).

As to claims 15 and 20, Bean et al teach each of the retrieval channels are coupled to receive transfer extend entries and to provide (implicit: col. 7, lines 29-57) used read pointers to a first storage device of the peripheral device.

As per claim 17, Bean et al teach the transfer extend generator is coupled to the buffer memory to store the transfer extend entries (col. 4, lines 15-18).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Ellis et al and Bean et al because they both teach receiving and processing host commands for a data transfer between the host and the local memory and the Bean et al's teaching of the command queuing engine generating transfer extend entries for host commands would increase efficiency of the Ellis et al's microprocessor.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis et al., US patent No. 6,029,226 and Krakirian, US patent No. 5,781,803.

As to claim 4, Ellis et al teach a peripheral device (col. 4, lines 38-58) that includes a data controller, microprocessor, a buffer memory, local memory and a storage medium, and that is couplable to a host, wherein the data controller creates (col. 6, lines 17-33) threads of plurality of commands (merging of two host commands into a single disk command) and generates interrupt

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at the beginning (col. 3, lines 5-8; col. 6, lines 6-10) of the plurality of commands relative to a data transfer.

However, Ellis et al do not explicitly disclose generating interrupt at the end of the plurality of commands relative to a data transfer.

Krakirian teaches a peripheral device (fig. 3; col. 7, lines 8-25) that includes a data controller, microprocessor, a buffer memory, local memory and a storage medium, and that is couplable to a host. Specifically, Krakirian teaches a peripheral device for transferring data according to a SCSI command received from the host and for generating (col. 4, lines 4-43) interrupt to the microprocessor at the beginning and end of the command relative to a data transfer.

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Ellis et al and Krakirian because they both teach a peripheral device for transferring data according to a SCSI command received from the host and the Krakirian's teaching of generating interrupt at the end of the command would increase flexibility in SCSI command process of the microprocessor providing status and command complete message (Ellis et al: col. 2, lines 48-51 and Krakirian: col. 4, lines 40-43).

### *Conclusion*

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9. Any inquiry concerning this communication should be directed to Ilwoo Park, whose telephone number is (703) 308-7811 or via E-mail, *ilwoo.park@uspto.gov*. The Examiner can normally be reached Monday through Friday from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Thomas C. Lee, can be reached at (703) 305-9717.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 308-9051 (for formal communications intended for entry)

**or:**


(703)305-3718 (for informal or draft communications, please label

"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

  
Ilwoo Park

May 8, 2001

  
THOMAS LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100